Hardware Sizing and Specification

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Hardware Specification Methodology

The system hardware specification process includes the following steps:

- Gathering all requirements (includes performance modeling)
- Identifying all options and performing trade-offs
- Validating the specification
- Documenting the specification

These steps are performed iteratively until solutions are found which optimally satisfy constraints

System Level Requirements

System Level Requirements may impact system hardware specification:

- **Performance ==> processing, I/O and memory must be selected to meet performance needs**
- **Phasing ==> hardware procurement must be phased to meet requirements**
- **RMA ==> may be met through implementation of failover pairs, sparing, use of replication techniques, etc.**
- **Scalability ==> must enable system growth without redesign (as specified in Level 3s for subsystems)**
- **Evolvability ==> must enable migration to new technologies**
- **Interoperability ==> may preclude the use of proprietary technologies**

Derived Requirements

Requirements derived from modeling and/or benchmarking include:

- **Computing throughput (MIPS, MFLOPS)**
- **Random Access Memory (MB)**
- **Virtual Memory (MB)**
- **Network throughput (Mbps)**
- **Number of Robots**
- **Number of Read/Write Stations**
- **Disk Space (GB)**
- **Disk I/O (MB/sec)**

Inputs to modeling include the ECS Technical Baseline, vendor specifications, benchmark results, and analysis of custom software

Modeling / Sizing Approaches

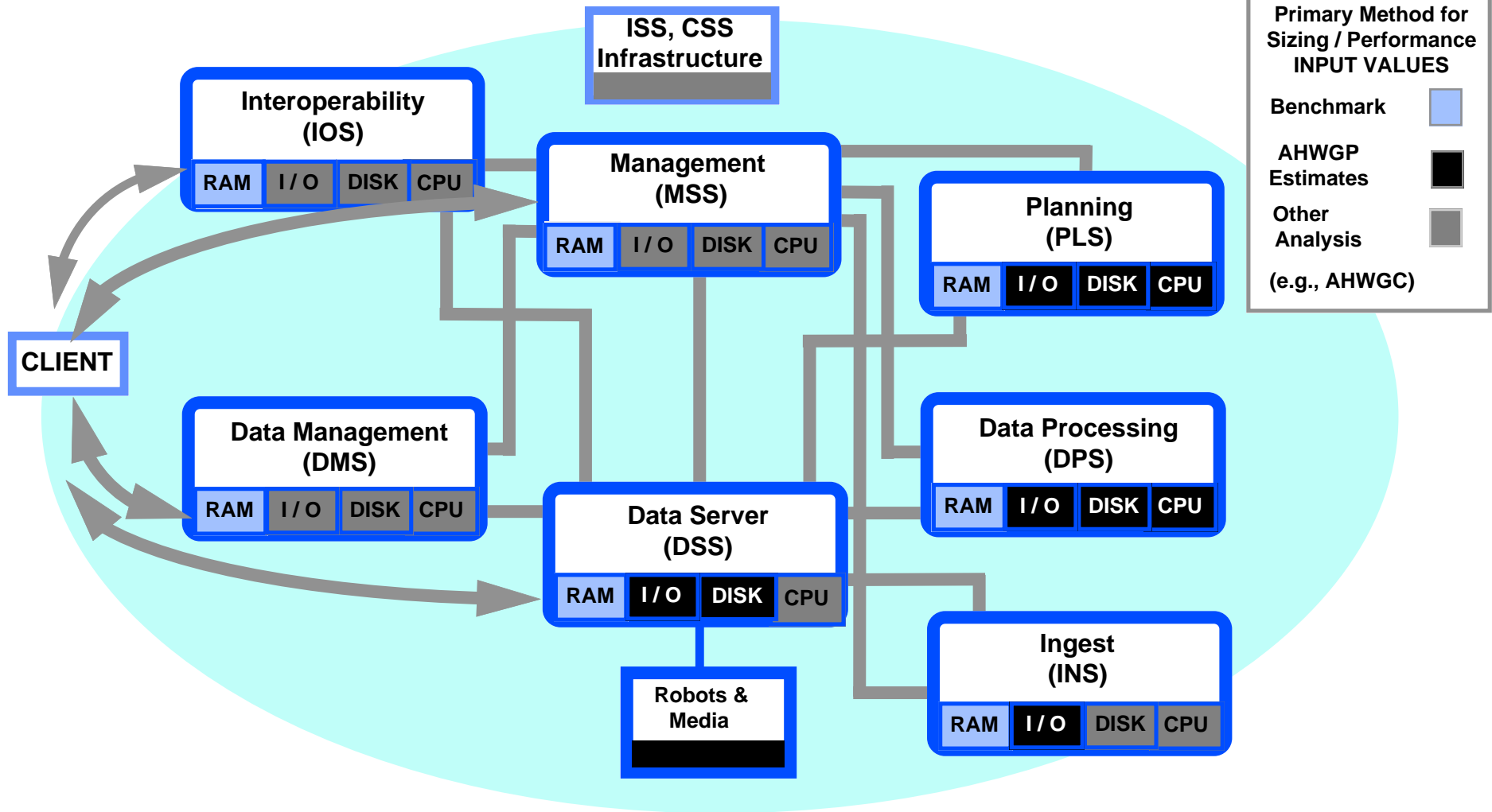The *Static Model* of AHWGP inputs provides coarse system sizing for production and data server systems.

The *ECS Dynamic Model* simulates the work done to process and store ECS products. It provides significant detail about peak resource requirements.

Subsystem-specific models and analyses are used to derive details about requirements for specific configurations (e.g., specifics of the archive configuration).

The *ECS End-to-End Model* is a queuing model used to analyze all ECS subsystems, using scenarios that take into consideration the system requirements and the candidate hardware design.

Benchmarks/Prototypes are used to measure the resource usage of COTS products and developed software as they will be used in the DAAC.

Modeling and Sizing Input Values

Primary Method for Sizing / Performance INPUT VALUES

Benchmark

AHWGP Estimates

Other Analysis

(e.g., AHWGC)

ISS, CSS Infrastructure

Interoperability (IOS)

| RAM | I / O | DISK | CPU |

Management (MSS)

| RAM | I / O | DISK | CPU |

Planning (PLS)

| RAM | I / O | DISK | CPU |

CLIENT

Data Management (DMS)

| RAM | I / O | DISK | CPU |

Data Server (DSS)

| RAM | I / O | DISK | CPU |

Data Processing (DPS)

| RAM | I / O | DISK | CPU |

Robots & Media

Ingest (INS)

| RAM | I / O | DISK | CPU |

Hardware Design Briefings

For each subsystem, we will describe:

- **Driving requirements**

- **Sizing approach (modeling, analysis, benchmarks)**

- **Hardware configuration**

  - **Computing platforms (make, model, number of CPUs, I/O configuration, memory)**

  - **Storage (RAID, disk, tape libraries)**

  - **Networks (protocols, selection of devices, topology, security, addressing)**

  - **Specific example of LaRC, EDC or GSFC**

- **Failover and RMA considerations**

- **Scalability: "breakpoint analysis"**

Hardware Sizing / Modeling Agenda

Introduction (Mary Armstrong)	**8:00 - 8:15**
Subsystem Designs	
• **Production (Randy Miller)**	**8:15 - 9:15**
• **Planning and Scheduling (Gary Roth)**	**9:15 - 9:45**
• **Data Server (Alla Lake)**	**9:45 - 10:45**
• **Ingest (Carey Gire)**	**10:45 - 11:15**
• **Interoperability, Data Management, Advertising (Richard Hunter)**	**11:15 - 11:30**
• **MSS / CSS (George Mellis)**	**11:30 - 12:00**
• **Networks (Ezra Jalleta)**	**1:00 - 1:45**
End-to-End Modeling (Singer)	**2:00 - 2:30**
Hardware Procurement (Mary Armstrong)	**2:30 - 3:00**